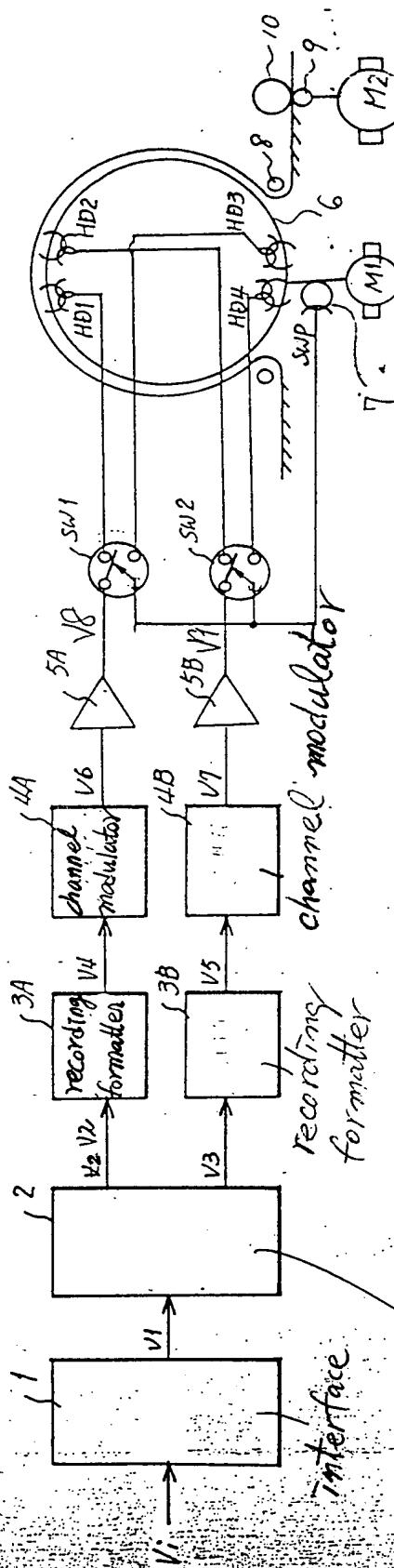


Fig. 1



interleaving and channel-dividing circuit

Fig. 3

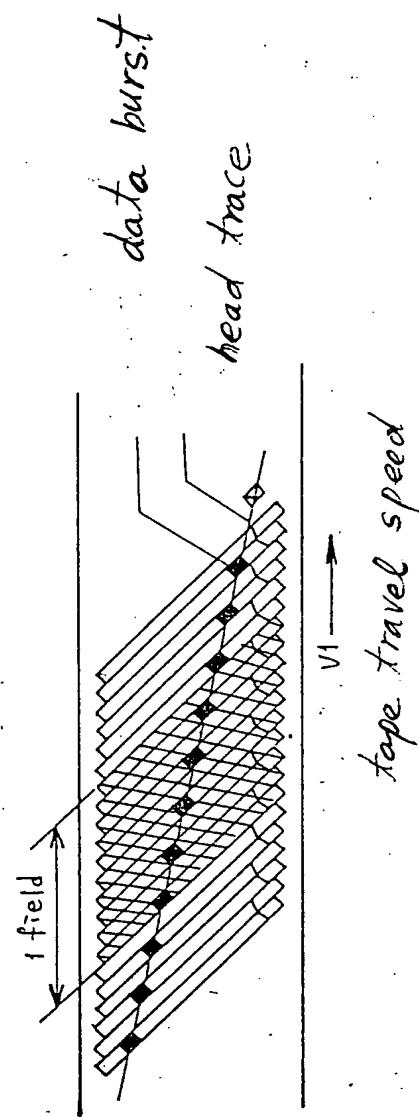


Fig. 2 Sync-detecting error-correcting circuit

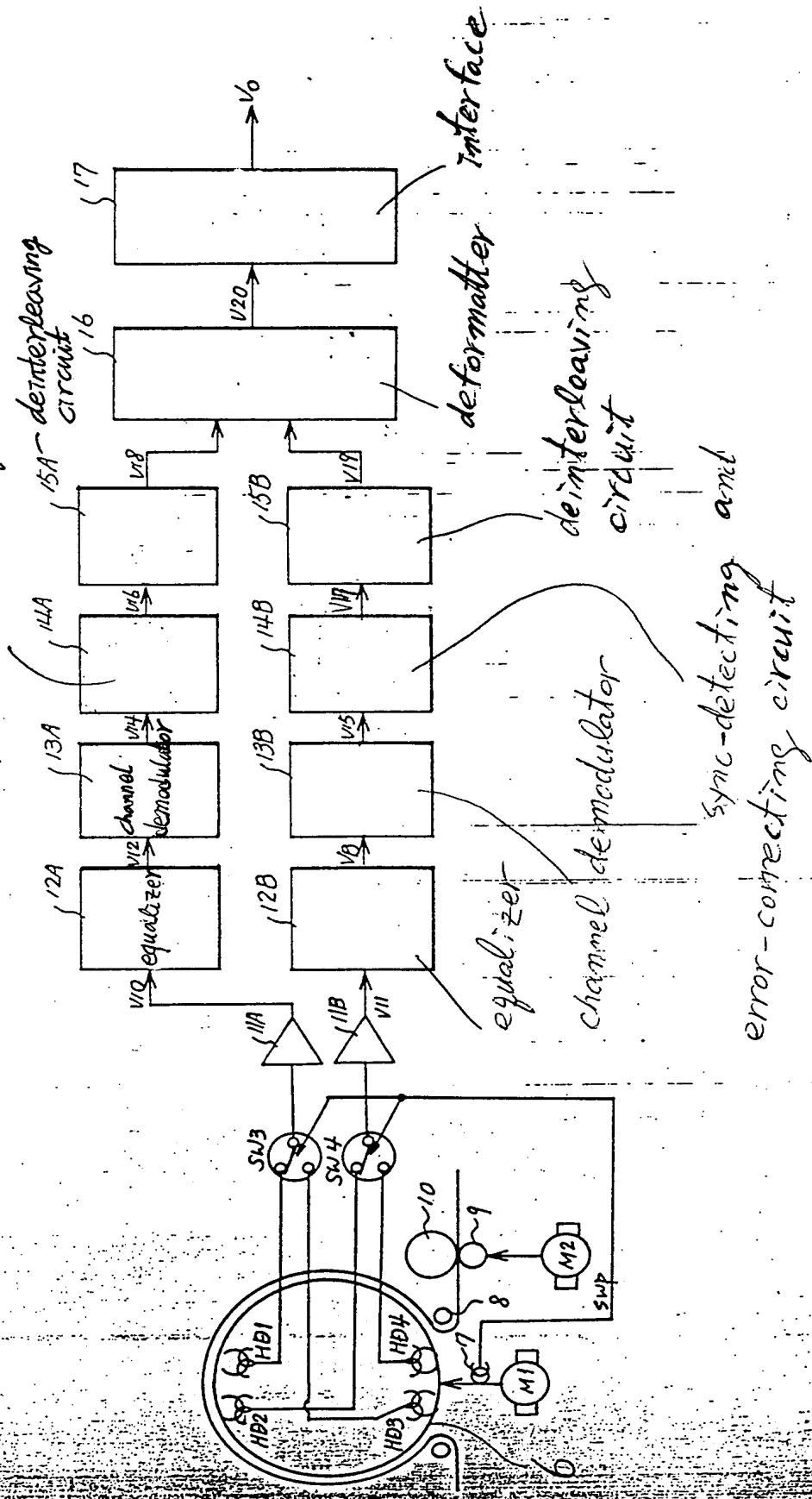


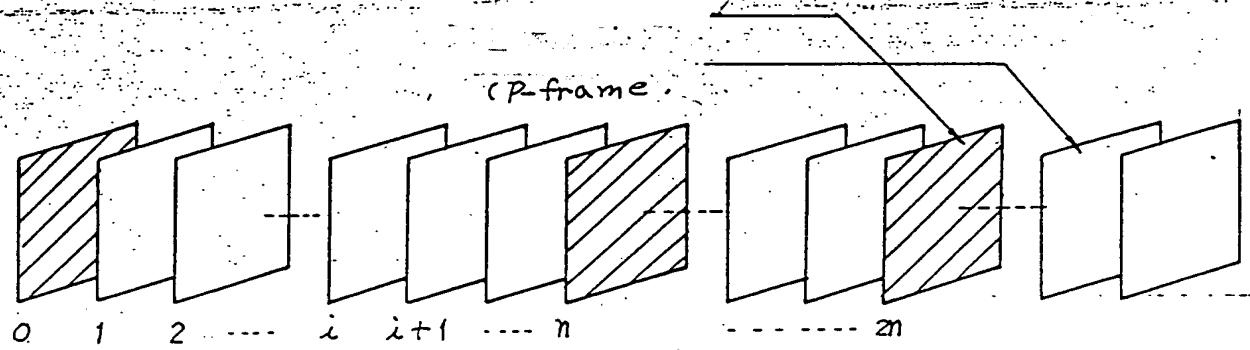
Fig. 4
I-frame

Fig. 5

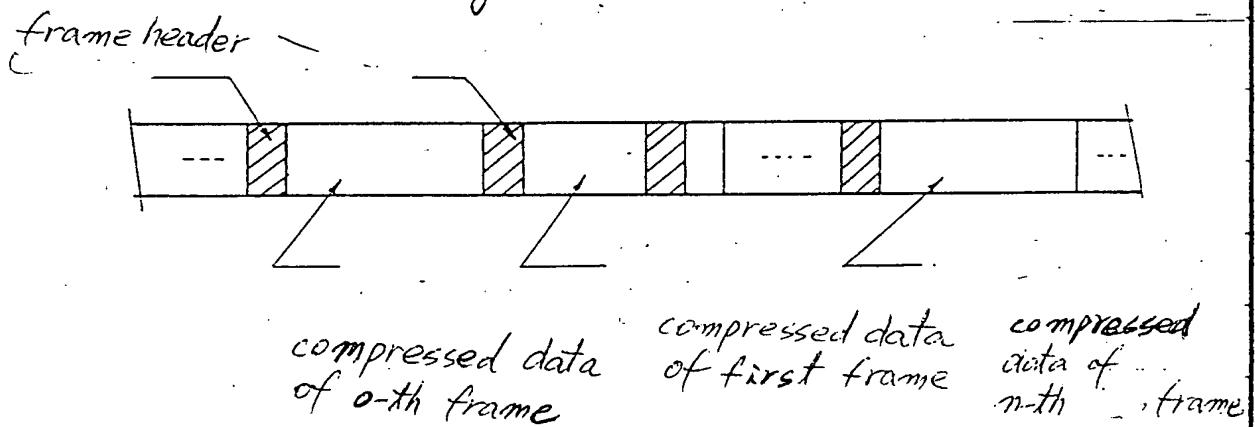


Fig. 6

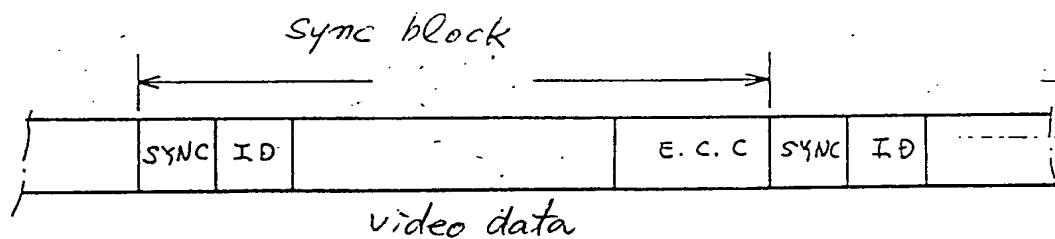


Fig. 7 interleaving and channel-division recording formatter circuit

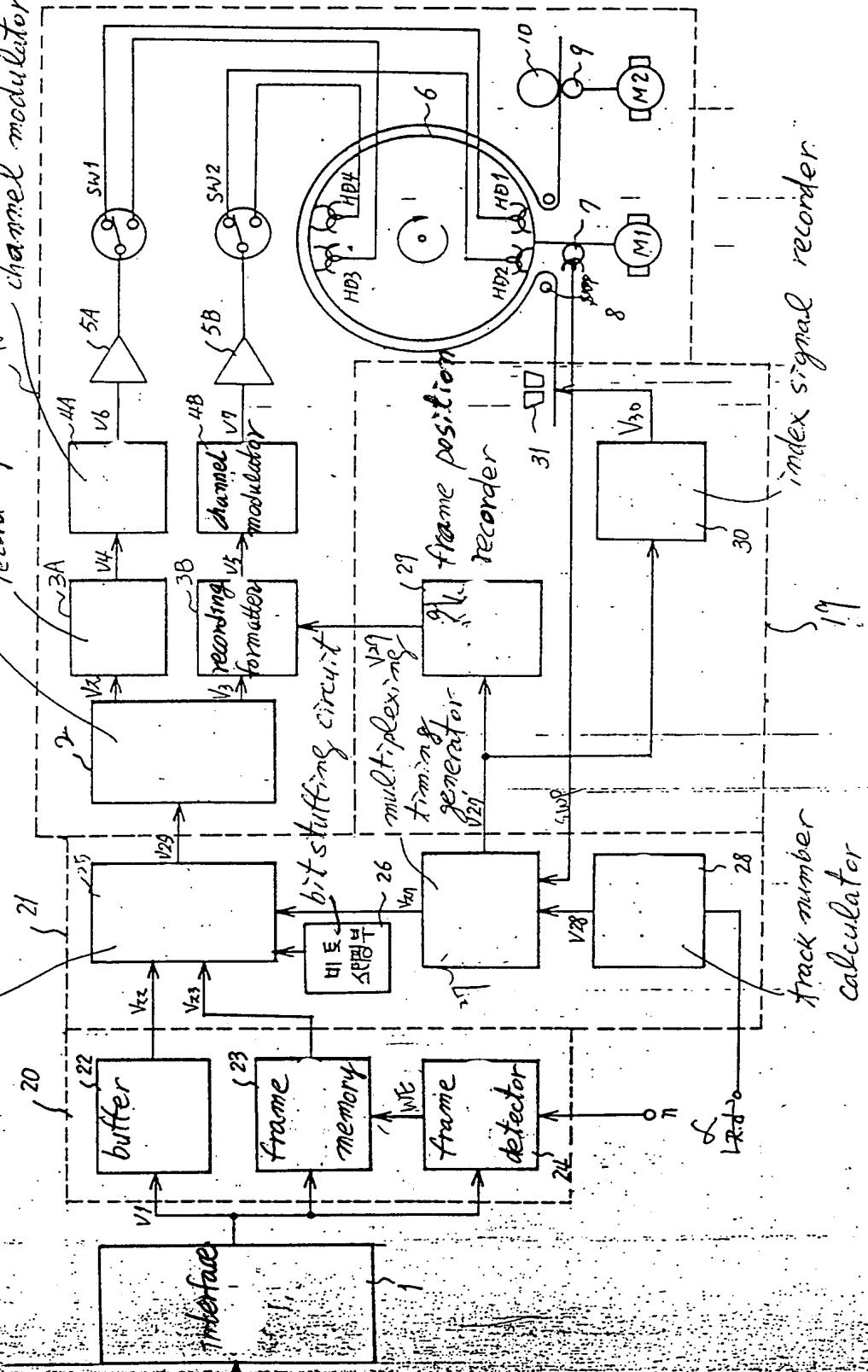
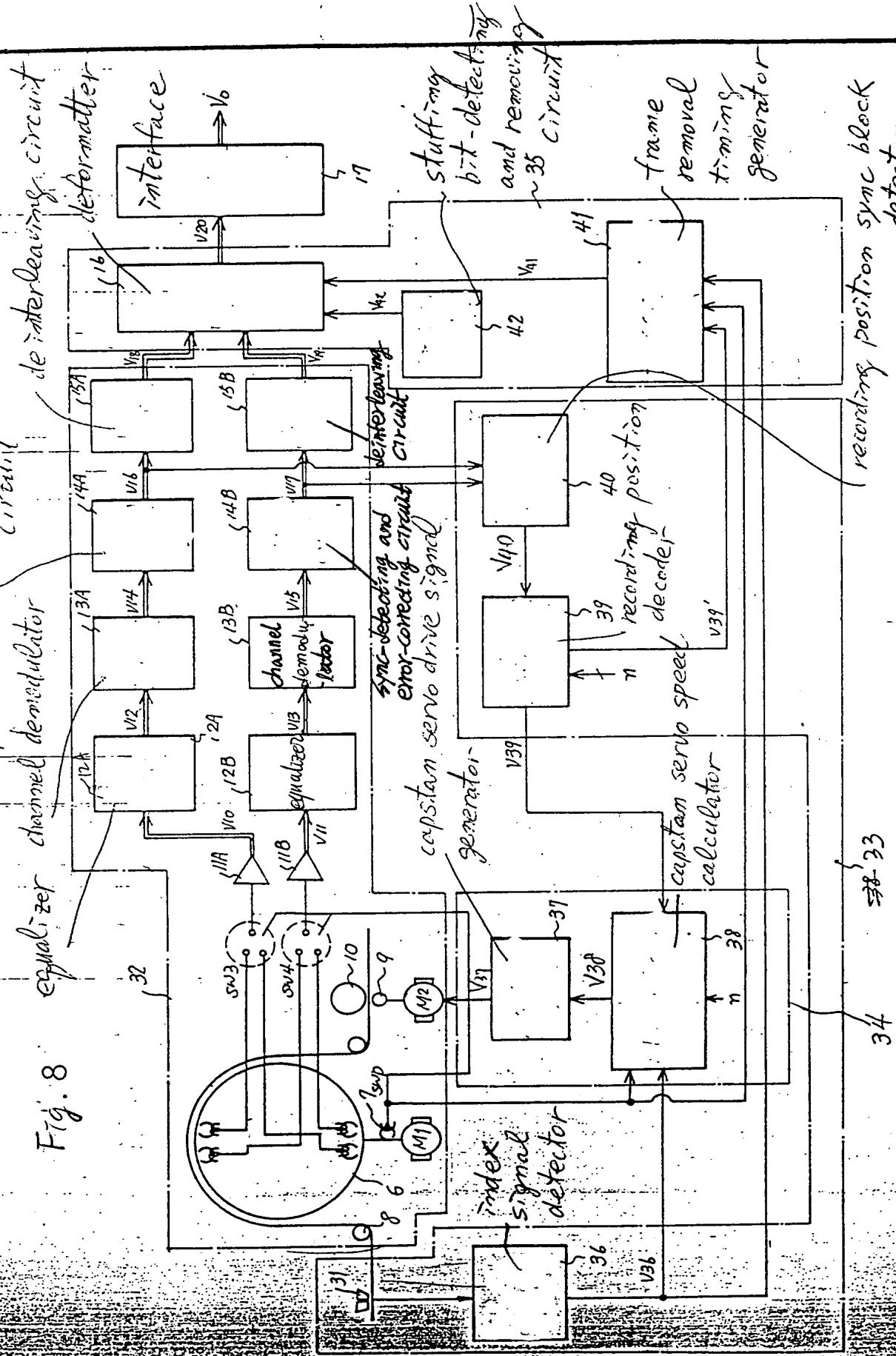
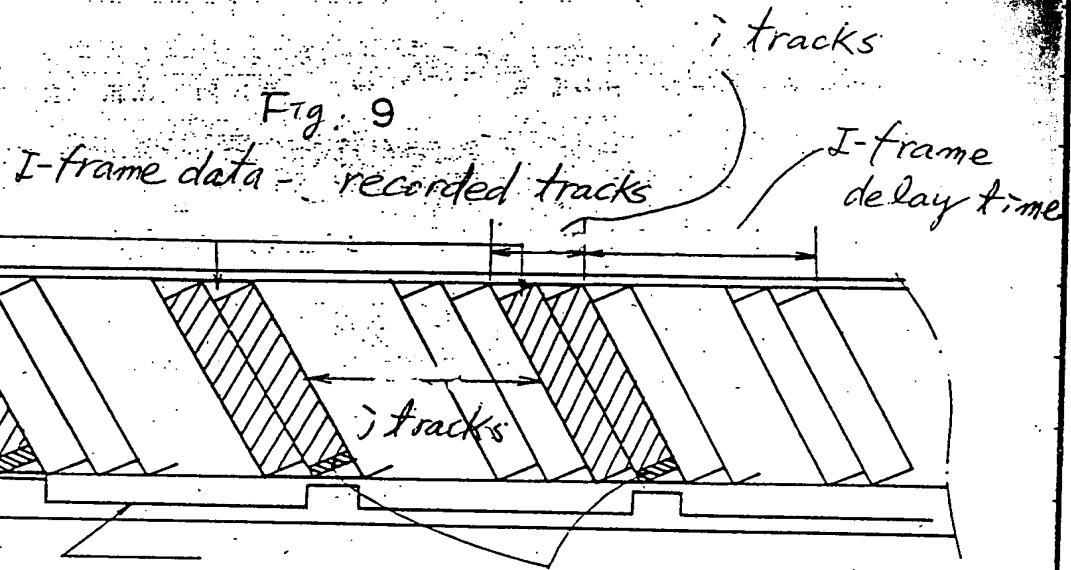


Fig. 8
sync-detecting and error-correcting
circuit





index information I-frame position
information sync
block

Fig. 10

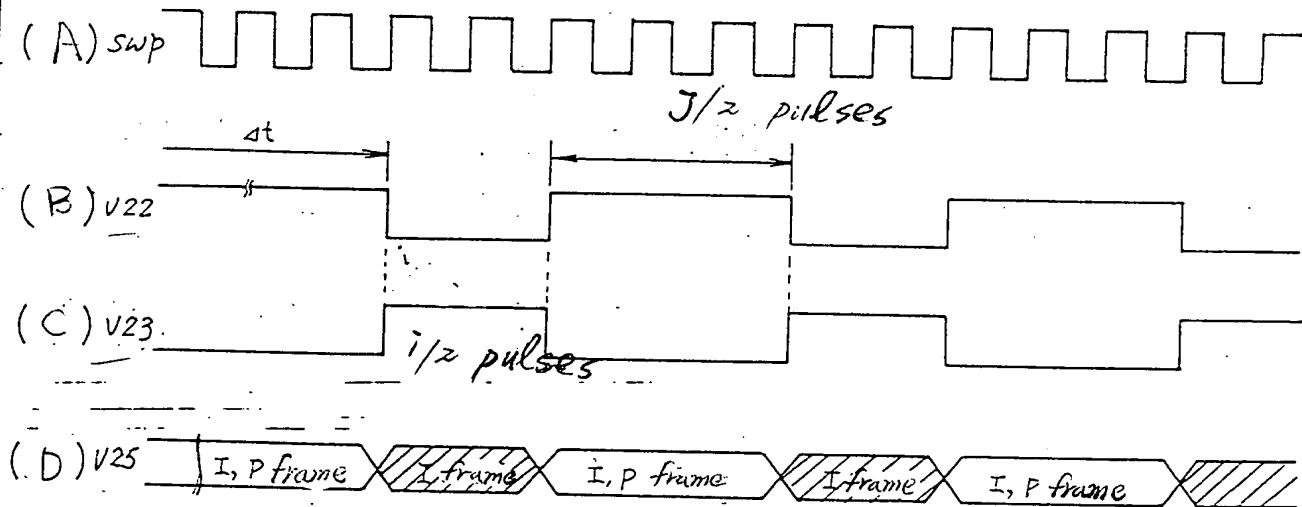
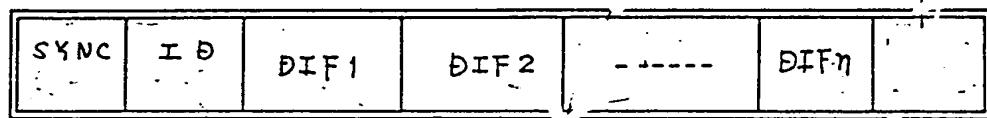


Fig. 11



* note: DIF 1 : code indicative of number of tracks present between current track and next track including specific data.

DIF 2 : " second track "

DIFn : " n-th track "

Fig. 12

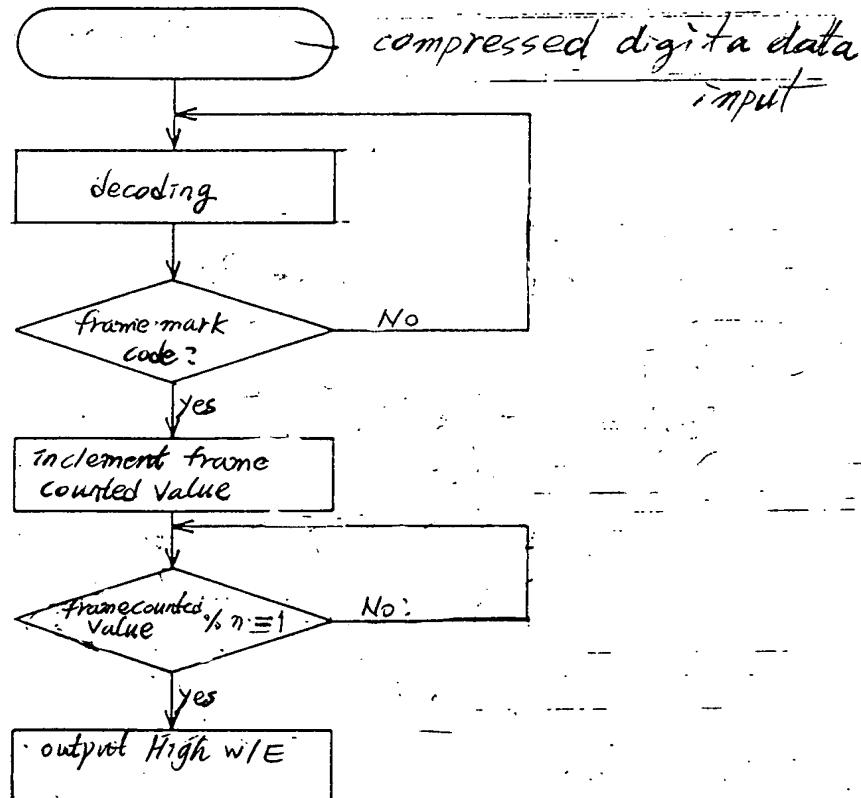


Fig. 13

travel (tracks)

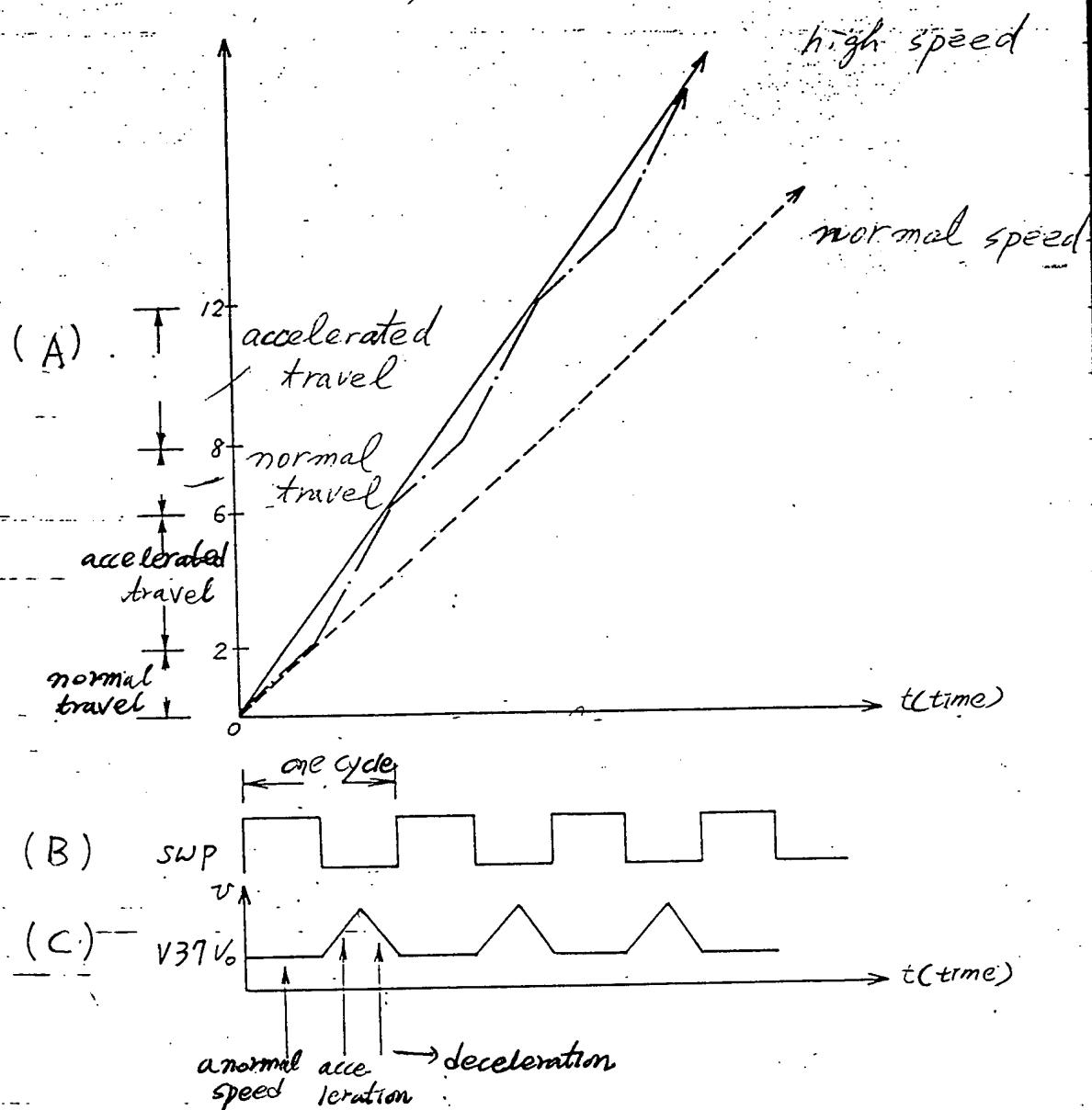


Fig. 14

